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06EC56

Fifth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Fundamentals of CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the working of enhancement mode transistor with neat nMOSFET structures at different conditions of applied voltages. Also draw the o/p characteristics and identify the different regions of operation. **(08 Marks)**

b. How many mask layers are required in a basic nMOS process? Explain the function of each of these masks. **(07 Marks)**

c. What is a noise margin? Obtain the values of V_{IL}, V_{IN}, V_{OI} and V_{OH} from transfer characteristics of a typical inverter. **(05 Marks)**

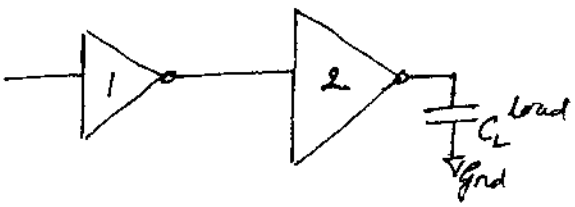
2 a. Explain λ-based design rules for contact cuts and vias with neat diagrams. **(12 Marks)**

b. Draw the stick diagram for the CMOS implementation of the Boolean expression $\overline{Y} = AB + C$. **(08 Marks)**

3 a. Explain the working of dynamic CMOS logic with necessary diagram and waveforms. What are the problems encountered in this logic? Explain how CMOS domino logic eliminates the above drawbacks with necessary diagrams. **(10 Marks)**

b. Discuss the working, merits and demerits of the following logic structures with two input NAND gate realization as an example: i) Complementary CMOS logic; ii) Pseudo NMOS logic. **(10 Marks)**

4 a. Two nMOS inverters are cascaded to drive capacitive load $C_L = 16 \square C_g$ as in Fig.Q.4(a). Calculate the pair delay (V_{in} to V_{out}) in terms of τ for the inverter geometry indicated in figure. What are the ratios of each inverter? If strays and wirings are allowed for, it would be reasonable to increase the capacitance to ground across the o/p of each inverter by $4 \square C_g$. What is the pair delay allowing for strays? Assume τ = 0.1nsec to evaluate this pair delay. **(08 Marks)**



Inverter 1	Inverter 2
$L_{pu} = 16\lambda$	$L_{pu} = 2\lambda$
$W_{pu} = 2\lambda$	$W_{pu} = 2\lambda$
$L_{pd} = 2\lambda$	$L_{pd} = 2\lambda$
$W_{pd} = 2\lambda$	$W_{pd} = 8\lambda$

Fig.Q.4(a)

b. What is the problem encountered in driving a large capacitive load? How this problem can be overcome using cascaded inverters? Obtain the expression for total delay for N stages of nMOS and CMOS inverters in terms of width factor f and delay τ. What is the problem encountered in cascaded inverters? Explain how it is overcome. **(12 Marks)**

PART – B

5 a. What are the two basic ways of building logic circuits? Explain each of them with an example each. Mention their advantages and disadvantages. **(10 Marks)**

b. When do you prefer to use MOS transistor drivers over bipolar drivers? Which are the three classes of MOS transistor bus systems? Explain each of them with essential diagrams. **(10 Marks)**

6 a. Explain the general design procedure for a 4-bit arithmetic processor with the floor plan for 4-bit data path. **(10 Marks)**

b. What are the basic requirement of a shifter? How a cross bar switch can be used as an shifter? Explain with an example of 4 × 4 cross bar switch. What are the drawbacks of this basic switch and how it is overcome? **(10 Marks)**

7 a. Explain the working of three transistor dynamic RAM cell with circuit and stick diagrams. **(10 Marks)**

b. What are timing considerations in system design? **(05 Marks)**

c. Describe the CMOS pseudo static D-flip-flop circuit. **(05 Marks)**

8 a. Discuss the difficulties encountered in testing sequential logic with an example. **(10 Marks)**

b. Write short notes on:

i) I/O pads.

ii) Real estate in VLSI design. **(10 Marks)**

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